In re Patent Application of
MAGNAVACCA ET AL.
Serial No. **Not Yet Assigned**
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In the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-3 (cancelled).

4. (new) A memory device comprising:

a plurality of memory chips assembled in a package and sharing input/output pins, the memory chips being singularly enabled by external commands; and

a single dedicated pin to receive an external enable/disable logic command;

each of the memory chips including

a plurality of primary input/output pads connected to the shared input/output pins,

a plurality of secondary input/output pads equal to 2*n, where 2^n is the number of memory chips of the device, and

a command circuit to generate an internal enable/disable command based upon logic inputs on the secondary pads and the external enable/disable logic command.

5. (new) The memory device according to Claim 4, wherein at least one of the plurality of secondary input/output pads of each memory chip is hardwired biased in a coordinated fixed logic state to distinguish each memory chip from the other(s), the other secondary input/output pad(s) are connected to receive at least one most significant bit from an external address bus.

6. (new) The memory device according to Claim 5, wherein each command circuit comprises input buffers coupled to the respective secondary input/output pads of the memory chip and a combinatory logic circuit to receive output signals of the buffers and the external enable/disable command for selecting the memory chip to which an addressed memory location pertains based upon the at least one most significant bit of the external address bus and the coordinated fixed logic states of the respective secondary input/output pads of the different memory chips.

7. (new) A memory device comprising:

a plurality of memory chips assembled in a package that includes a single dedicated pin to receive an external enable/disable logic command for the plurality of memory chips;

each of the memory chips including a command circuit, having a plurality of secondary input/output pads, to generate an internal enable/disable command based upon signals received at the secondary input/output pads and the external enable/disable logic command received at the single dedicated pin.

8. (new) The memory device according to Claim 7 wherein the plurality of secondary input/output pads comprise 2*n secondary input/output pads, where 2^n is the number of memory chips of the device.

9. (new) The memory device according to Claim 7, wherein at least one of the secondary input/output pads of

each memory chip is hardwired biased in a coordinated fixed logic state to distinguish each memory chip from the other(s).

10. (new) The memory device according to Claim 9, wherein the other secondary input/output pad(s) are connected to receive at least one most significant bit from an external address bus.

11. (new) The memory device according to Claim 10, wherein each command circuit comprises input buffers coupled to the respective secondary input/output pads of the memory chip and a combinatory logic circuit to receive output signals of the buffers and the external enable/disable command for selecting the memory chip to which an addressed memory location pertains based upon the at least one most significant bit of the external address bus and the coordinated fixed logic states of the respective secondary input/output pads of the different memory chips.

12. (new) A method of making a memory device comprising:

packaging a plurality of memory chips in a package that includes a single dedicated pin to receive an external enable/disable logic command for the plurality of memory chips;

providing each of the memory chips with a command circuit, having a plurality of secondary input/output pads, to generate an internal enable/disable command based upon signals received at the secondary input/output pads and the external enable/disable logic command received at the single dedicated pin.

13. (new) The method according to Claim 12 wherein the plurality of secondary input/output pads comprise 2*n secondary input/output pads, where 2^n is the number of memory chips of the device.

14. (new) The method according to Claim 12, wherein at least one of the secondary input/output pads of each memory chip is hardwired biased in a coordinated fixed logic state to distinguish each memory chip from the other(s).

15. (new) The method according to Claim 14, wherein the other secondary input/output pad(s) are connected to receive at least one most significant bit from an external address bus.

16. (new) The method according to Claim 15, wherein each command circuit comprises input buffers coupled to the respective secondary input/output pads of the memory chip and a combinatory logic circuit to receive output signals of the buffers and the external enable/disable command for selecting the memory chip to which an addressed memory location pertains based upon the at least one most significant bit of the external address bus and the coordinated fixed logic states of the respective secondary input/output pads of the different memory chips.